Ceres and Oberon – Then and Now

Oberon-Day ETH, 27 May 2011 Niklaus Wirth

25 years ago Motivation and Purpose

- Return from a sabbatical at Xerox PARC
- Charged of teaching a course about Operating System Design
- Need for becoming familiar with the topic
- Commercial systems neither transparent, nor explicable, nor exemplary
- Design your own! ③

A small team

- J. Gutknecht & N. Wirth
- The Language Oberon, a lean derivative of Pascal and Modula-2
- The System: A descendant of Xerox' Cedar, reduced to basics and essentials
- The Hardware: First version implemented on Lilith, then transferred to Ceres

Ceres (1986)

- Processor with the first 32-bit microprocessor chip of National Semiconductor NS32032
- 10 MHz clock rate
- 4 Mbyte memory
- 40 Mbyte disk (later 80 MB)
- Bit-mapped display with 1024 x 800 pixel
- Mouse, keyboard
- RS-485 network, RS-232 serial link
- 3.5" diskette

The Oberon System

- File system
- Viewer system
- Text system
- Task system

not hierarchical not overlapping not object-oriented not interruptible

Basic philosophy: Concentrate on what is essential

Omit temptations for bells and whistles

All designed in the same language: Oberon

Education in Focus

- Teach understanding, rather than details
- Commercial systems totally unsuitable
- Too huge, therefore inappropriate
- Too intricate and intransparent
- Cancerous growth, hard to justify (Except for commercial reasons?)
- Must be able to explain principles
- Must be able to separate concerns

2011

- These objections and shortcomings still hold 25 years later. In fact, even more so.
- Why are systems so complex?
- Lack of design discipline; abundant hardware fosters waste and inefficiency.
- Oberon was described in its entirety in a single book (Project Oberon, 1992)
- Therefore a new look at Oberon's philosophy seems appropriate now.

Extending the idea to hardware

- Compiler Construction (Wirth, 1976, 1995)
- Language: $PL0 \rightarrow Oberon0$
- Target computer: Stack computer \rightarrow RISC
- 2011: RISC slightly extended and implemented on FPGA, specified in Verilog
- Available on low-cost development board Xilinx Spartan-3